WO 2004/093324 PCT/IB2004/050424

10

CLAIMS:

5

15

20

1. A unit (100, 101, 200, 201, 301) comprising:

n (n \geq 1) integrators (I_{1...n}) in series, a first of the n integrators (I_{1...n}) receiving an input signal;

at least one device (Q), which acts as a quantizer when an absolute value of a signal input thereto is smaller and as a gain element when the absolute value of the signal input thereto is larger; and

a device (12) for quantizing an output of the unit (100, 101, 200, 201, 301).

- 2. The unit (100, 101 200, 201, 301) of claim 1, wherein the at least one device acts as a gain device, with or without an offset.
 - 3. The unit (100) of claim 2, wherein the signal input to the at least one device (Q_1) is an output of the integrator (I_n) and the output of the at least one device (Q_1) is input to the device 12 and as weighted feedback paths to the n integrators $(I_{1...n})$.

4. The unit (100) of claim 2, wherein the signal input to the at least one device (Q_1) is an output of the integrator (I_n) and the output of the integrator (I_n) is input to the device (12), and the output of the at least one device (Q_1) is input to the weighted feedback paths to the n integrators $(I_{1...n})$.

5. The unit (101) of claim 2, wherein the signals output from the n integrators $I_{1...n}$ are weighted and summed and the summed output is input to the at least one device (Q_1) an output of the at least one device (Q_1) is input to the device (12) and to integrator (I_1) .

25 6. The unit (101) of claim 2, wherein the signals output from the n integrators (I_{1...n}) are weighted and summed and the summed output is input to the at least one device (Q₁) and the device (12), and an output of the at least one device (Q₁) is input to the integrator (I₁).

WO 2004/093324 PCT/IB2004/050424

7. The unit (200) of claim 2, wherein the signal input to the at least one device $(Q_{1...m})$ where $m \le n$, is an output of the integrator (I_n) , the outputs of the at least one device $(Q_{1...m})$ is input as weighted feedback paths to one or more of the n integrators $(I_{1...n})$ and an output of the integrator (I_n) is input to the device (12).

8. The unit (200) of claim 2, wherein the signal input to the at least one device $(Q_{1...m})$, is an output of the integrator (I_n) , the outputs of the at least one device $(Q_{1...m})$ is input as weighted feedback paths to one or more of the n integrators $(I_{1...n})$ and the output of any of the at least one devices $(Q_{1...m})$ is input to device (12).

5

10

15

20

25

30

- 9. The unit (201) of claim 2, wherein the signals output from the n integrators $(I_{1...n})$ are weighted and summed, the summed output is input to the at least one device $(Q_{1...m})$ outputs of the at least one device $(Q_{1...m})$ is input to one or more of the n integrators $(I_{1...n})$, and an output of one of the at least one device $(Q_{1...m})$ is input to the device (12).
- 10. The unit (201) of claim 2, wherein the signals output from the n integrators $(I_{1...n})$ are weighted and summed, the summed output is input to the at least one device $(Q_{1...m})$, outputs of the at least one device $(Q_{1...m})$ are input to one or more of the n integrators $(I_{1...n})$, and the summer (13) output is input to the device (12).
 - The unit (301) of claim 2, wherein the signals output from the n integrators $(I_{1...n})$ are weighted and summed, the summed output is input to the at least one device $(Q_{1...m})$ and the device (12), and outputs of the at least one device $(Q_{1...m})$ is input to one or more of the n integrators $(I_{1...n})$.
 - 12. The unit (301) of claim 2, wherein the signals output from the n integrators $(I_{1...n})$ are weighted and summed, the summed output is input to the at least one device $(Q_{1...m})$, and outputs of the at least one device $(Q_{1...m})$ are input to one or more of the n integrators $(I_{1...n})$ and an output of one of the at least one device $(Q_{1...m})$ is input to device (12).
 - 13. An analog to digital converter including the unit (100, 101, 200, 201, 301) of any the preceding claims.

WO 2004/093324 PCT/IB2004/050424

12

- 14. A digital to digital converter including the unit (100, 101, 200, 201, 301) of claims 1-12.
- The unit (100, 101, 200, 201, 301) of any of claims 1-12, wherein each of the
 m devices (Q_{1...m}) has different parameters set to improve stability, improve SNR, and/or reduce introduction of artifacts.
- 16. A method, comprising:
 inputting a signal to n (n≥1) integrators (I_{1...n}) in series; and
 quantizing when an absolute value of a signal input thereto is smaller and
 amplifying, with or without offset, when the absolute value of the signal input thereto is
 larger; and

quantizing an output.